UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/827,056	04/03/2001	Chun-Mai Liu	16405-0013	3447

20350 7590 08/12/2004

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
MAGEE, THOMAS J	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 08/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO 90C (Rev 10/03)

Office Action Summary	Application No.	Applicant(s)
	09/827,056	LIU ET AL.
	Examiner	**Art Unit**
	Thomas J. Magee	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _09 October 2002_ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-14, 16_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-14 and 16_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Reopening of Prosecution

1. In view of the Appeal Brief filed on April 19, 2004, PROSECUTION IS HEREBY RE-OPENED. New grounds of rejection are set forth below. To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Drawing Objections

2.The drawings are objected to under 37 CFR 1.83(a) because they fail to show, as described in the specification, "*a first gate oxide layer 142 formed over the exposed portions of the silicon substrate 42, over a portion of the floating gates 124 and over the floating gate oxide layer 132*" wherein "*a nitride layer is deposited over the first oxide layer 142.*" Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections – 35 U.S.C. 103

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 103(a) which form the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 5, 9, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,355,527) in view of Brower (US 4,212,684).

5. Regarding Claim 1, Lin et al. disclose a method for forming split-gate flash memories, comprising:

providing a silicon substrate (Col.5, line 34) (Figure 2A) having a top surface,

forming a common source region (125) (Figure 2G) in an area of the top surface for each pair of cells,

forming floating gates (140) (Figure 2D) overlying areas of the predefined (source) region (Figure 2G),

forming select gates (160) with extremities extending over the floating gate, and

forming drain regions (120) positioned proximate an extremity of one of the select gates.

Lin et al. do not disclose forming a common source region in an area of the top surface for each pair of cells and implanting ions into predefined areas of each common source region <u>prior to fabrication of floating gate structure.</u> However, Brower discloses formation of an FET for a memory device, wherein, photoresist masking is done and source (drain) (n+) and

threshold (p) implants (Figures 1 and 3) performed prior to forming the gate electrode. It would have then been obvious to one of ordinary skill in the art at the time of the invention to use the implant sequence of Brower to form common source regions with subsequent channel implants (25) performed to adjust threshold voltage, and the gate formation procedures of Lin et al. to obtain a split gate flash memory cell with improved control of ion implanted source and channel regions.

6. Regarding Claim 2, Lin et al. do not disclose the fabrication steps for forming a common source region on the substrate, wherein "predefined" areas are defined. Brower discloses the formation of the source region including the steps of:

patterning a photoresist deposited to define predefined areas at which source is to be formed (Col. 4, lines 38 – 41, 54 – 57),

implanting ions into substrate, where the resist has been used as a mask (Col. 4, lines 61 – 63), and

the photoresist removed (Col. 4, lines 59 – 61).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the procedures of Brower in forming ion implanted regions in predefined regions with Lin et al. to obtain a split gate flash memory cell with improved control of ion implanted source regions.

7. Regarding Claim 5, Lin et al. disclose a method of forming floating gates, including the steps of:

forming a tunneling oxide (130) (Figure 2B) over the top surface of substrate,

depositing a first polysilicon layer (140) (Col. 6, line 13) over the oxide,

depositing a nitride masking layer (143) (Figure 2B) over the polysilicon,

patterning and etching nitride layer to expose first and second polysilicon regions (Col. 5, lines 62 – 66), wherein said exposed regions define first and second floating gate regions (Figure 2D),

forming a floating gate oxide layer (145) (Col. 6, lines 3 – 8) over the polysilicon,

removing the nitride masking layer (Col. 6, lines 8 – 10), and

etching first polysilicon layer using the oxide layer (145) as a mask (Col. 6, lines 10 – 14) wherein the tunnel oxide is disposed beneath the floating gate oxide, sidewalls (Figure 2G) are present

Lin et al. do not disclose implanting ions into the gate regions (channel) to adjust threshold voltage. Brower discloses the implanting of ions (Col. 5, lines 31 – 35) into the gate (channel) area. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Brower with Lin et al. to obtain a working device with an optimized threshold voltage.

8. Regarding Claim 9, Lin et al. do not disclose the implantation of boron ions for threshold adjustments. As discussed above, Brower discloses the use of boron ion implantation into predefined regions (Figure 3) to adjust threshold voltage (Col. 5, lines 31 – 38). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Brower with Lin et al. to obtain a working device with an optimized threshold voltage.

9. Regarding Claims 12 and 13, Lin et al. disclose the formation of a polysilicon layer using LPCVD with a SiH4 source at a temperature of 550 to 600 degrees (C) to a thickness between about 1500 to 2500 Angstroms (Col. 6, lines 58 – 62). These are in the range of values recited in the instant application.

10. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Brower, as applied to Claims 1, 2, 5, 9, 12, and 13 above, and further in view of Sze ("Physics of Semiconductor Devices," John Wiley & Sons, New York (1981), p. 68).

Although both Lin et al. and Brower disclose (Col. 6, lines 42 – 45) the implantation of phosphorus, both arsenic and phosphorus are n-type implants and either could be used. The diffusion coefficients of these n-type dopants are well known in the art (See Sze, page 68) and differences in lateral and/or vertical diffusion lengths can be readily calculated and implant conditions altered accordingly.

11. Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Brower, as applied to Claims 1, 2, 5, 9, 12, and 13 above, and further in view of Wolf et al. ("Silicon Processing for the VLSI Era: Volume 1 – Process Technology," Lattice Press, Sunset Beach, CA (1986), pp.321 – 322) and Brower.

12. Regarding Claim 4, as discussed earlier, Lin et al. disclose the the use of patterned photoresist on a dielectric for ion implantation masking, followed by removal of the dielectric and photoresist from the surface of the substrate. Although the use of sacrificial oxides is not disclosed, thin oxide layers are routinely used as blocking (or screening) layers for ion implants (Wolf et al., pp. 321 – 322). Brower discloses (Col. 4, lines 29 – 36, 59 – 63)

(Col. 5, lines 6 – 8) the use of an oxide layer (24) (Fi9gure 1) and photoresist masking (not shown) to form source regions. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wolf et al. and Brower with Lin et al. to obtain a screening or blocking layer for the implant.

13. Regarding Claim 11, Lin et al. (Col. 6, lines 42 – 45) and Brower disclose the use of a phosphorus implant for forming the common source region, whereas, the instant application recites the use of an arsenic ion implant. However, both arsenic and phosphorus are n-type implants. It would have been obvious to one of ordinary skill in the art at the time of the invention that either could be used. The diffusion coefficients of these n-type dopants are well known in the art (See Sze, page 68) and differences in lateral and/or vertical diffusion lengths can be readily calculated and implant conditions altered accordingly.

14. Claims 6, 7, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Brower, as applied to Claims 1, 2, 5, 9, 12, and 13 above, and further in view of McGuire ("Semiconductor Materials and Process Technology Handbook," Noyes Publ., Norwich, N.Y. (1988), pp. 575 – 591).

15. Regarding Claim 6, Lin et al. disclose, as previously discussed, steps for forming select gates, including:

forming an insulating layer (130) (Figure 2D) over the substrate and a floating gate oxide layer (145) covering floating gates, and

forming a second polysilicon layer (160) (Figure 2G) over the insulating layer.

Lin et al. do not explicitly identify a conductive layer overlying the second polysilicon layer or patterning/removal of portions of the conductive layer and underlying structural elements to form a select gate. Conductive metal layers are well known in the art (See McGuire, pp. 575 -591) and it would have been obvious to one of ordinary skill in the art to add McGuire to Lin et al. to include a specific conductive metal layer with patterning/removal of portions thereof to complete a memory device.

16. Regarding Claim 7, Lin et al. disclose a method of forming an insulating layer over substrate, floating gate oxide layer covering the floating gate includes the steps of:

forming a first gate oxide layer (130) over the substrate

forming a nitride layer (Col. 8, lines 58 – 60) over first oxide layer (130),

performing an etching process to remove a portion of said nitride layer, leaving nitride spacers (170) adjacent the side walls of floating gates (Col. 7, lines 11 – 14) (Col. 8, lines 58 – 60), and

forming a second gate oxide layer (144) over the first oxide layer and floating gate oxide layer (145) and "over" nitride spacers (lateral edges).

It is assumed that the first gate oxide is formed (only) on the substrate, as shown in Figure 2E of the instant application.

17. Regarding Claim 10, Lin et al. disclose (Col. 7, lines 14 – 18) the formation of ion implanted drain regions, but do not explicitly teach the patterning and etching of a conducting film. As discussed earlier, it would have been obvious to add a conducting film layer to complete the device.

18. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Brower, and McGuire, as applied to Claims 1, 2, 5 - 7, 9, 10, 12, and 13, and further in view of Wilson et al. ("Handbook of Multilevel Metallization for Integrated Circuits," Noyes Publ., Westwood, New Jersey, (1993), p. 868).

Lin et al. do not disclose a tungsten conductive layer. Tungsten, however, has been routinely utilized in the art (Wilson et al., page 868, 1st paragraph) for plugs, inter-connects, and standard metallization levels. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to utilize Wilson et al. in forming tungsten conducting layers to obtain stable contacts, and to combine Wilson et al. with Wolf and Lin et al.

19. Claims 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Brower, Wolf, and McGuire.

20. Regarding Claim 14, Lin et al. disclose a process for fabricating a flash memory device having a high coupling ratio, comprising:

providing a silicon substrate (Col.5, line 34) (Figure 2A) having a top surface,

forming a tunneling oxide (130) (Figure 2B) over the top surface of substrate,

depositing a first polysilicon layer (140) (Col. 6, line 13) over the oxide,

depositing a nitride masking layer (143) (Figure 2B) over the polysilicon,

patterning and etching nitride layer to expose first and second polysilicon regions (Col.

5, lines 62 – 66), wherein said exposed regions define first and second floating gate regions (Figure 2D), with an overlying portion extending into the common source region (Figure 2G)

forming a floating gate oxide layer (145) (Col. 6, lines 3 – 8) over the polysilicon,

removing the nitride masking layer (Col. 6, lines 8 – 10),

patterning and etching nitride layer to expose first and second polysilicon regions (Col. 5, lines 62 – 66), wherein said exposed regions define first and second floating gate regions (Figure 2D), each floating gate having a substantial portion overlying the common source region (Figure 2G) with the common source region having a portion implanted with first ions, as discussed for Claim 1 (Brower, Figures 1 and 3),

implanting second ions into portions of the substrate defined by first and second floating gate regions and extremities of common source region to adjust threshold voltage, as discussed for Claim 5 (Brower, Col. 4, lines 54 – 62; Col. 5, lines 31 – 35),

etching first polysilicon layer using the oxide layer (145) as a mask (Col. 6, lines 10 – 14) wherein the tunnel oxide is disposed beneath the floating gate oxide, wherein sidewalls (Figure 2G) are present at the edges of floating gate

forming a floating gate oxide layer (145) (Col. 6, lines 3 – 8) over the polysilicon,

removing the nitride masking layer (Col. 6, lines 8 – 10),

etching first polysilicon layer using the oxide layer (145) as a mask (Col. 6, lines 10 – 14) wherein the tunnel oxide is disposed beneath the floating gate oxide, sidewalls (Figure 2G) are present with an overlying portion extending into the common source region (Figure 2G) increases the coupling ratio (Col. 7, lines 1 – 4).

forming a first gate oxide layer (130) over the substrate (It is assumed that the first gate oxide is formed (only) on the substrate, as shown in Figure 2E of the instant application),

forming a nitride layer (Col. 8, lines 58 – 60) over first oxide layer (130),

performing an etching process to remove a portion of said nitride layer, leaving nitride spacers (170) adjacent the side walls of floating gates (Col. 7, lines 11 – 14) (Col. 8, lines 58 – 60),

forming a second gate oxide layer (144) over the first oxide layer and floating gate oxide layer (145) and "over" nitride spacers (lateral edges),

forming a second polysilicon layer (Col. 6, lines 51 – 54) (160) (Figure 2G) over the second gate oxide layer (150),

implanting third ions into drain regions to form drains (120),

whereby the floating gate has an overlying portion extending into the common source region (Figure 2G) providing a high coupling ratio (Col. 7, lines 1 – 4).

Lin et al. do not disclose the formation of a sacrificial oxide atop the substrate. Thin oxide layers are routinely used as blocking (or screening) layers for ion implants (Wolf et al., pp. 321 – 322). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wolf et al. with Lin et al. to obtain a screening or blocking layer for an implant.

Lin et al. also do not disclose the patterning of a photoresist layer atop an oxide layer to define a common source region, followed by ion implantation and subsequent removal of photoresist and oxide. Brower discloses:

patterning a photoresist deposited to define predefined areas at which the common source is to be formed (Col. 4, lines 38 – 41, 54 – 57),

implanting ions into substrate, where the resist has been used as a mask (Col. 4, lines 61 – 63), and

the photoresist (Col. 4, lines 59 – 61) and oxide layer (Col. 5, lines 6 – 8) removed.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the procedures of Brower in forming ion implanted regions in predefined regions with Lin et al. to obtain a split gate flash memory cell with improved control of ion implanted source regions.

Further, Lin et al. do not disclose the formation of a conductive layer on the second polysilicon layer or the subsequent patterning and etching of underlying structure to form select gates with a portion overlying a portion of floating gate with lateral boundaries defining drain regions. However, conductive metal layers are well known in the art (See McGuire, pp. 575 – 591) as discussed in Claim 6, and it would have been obvious to one of ordinary skill in the art at the time of the invention to add McGuire to Lin et al. to include a specific conductive metal layer atop the polysilicon layer (Figure 2G, Lin et al.) with patterning and removal to form select gates with the lateral edge defining a drain region.

21. Regarding Claim 16, as discussed earlier for Claim 1, the first ion implant includes n-type ions and the second includes p-type ions, used for adjustment of threshold voltage (Brower, Figures 1 and 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the ion implantation of Brower in Lin et al. for formation of source regions and threshold voltage adjustment.

Response to Arguments

22. Applicant's arguments with respect to claims 1 – 14 and 16 in Letter of April 19, 2004 have been considered but these have been found to be unpersuasive. However, a few remarks can be made regarding the items. Applicant is correct in asserting (pp. 11 – 15) that there is an inferred chronology of process steps based on the prior amendment.

Since it has been shown that there is no explicit or implied teaching in the Specification demonstrating that the said (threshold) implant (boron) is used for <u>increasing the coupling ratio</u>, it is understood that the boron ions increase the coupling ratio, as taught by the reference.

With regard to Claim 4, the references when combined do indeed read upon the limitations of the claim.

With regard to Claim 8, the elements of the limitations of Claims 6 and 8 are well known in the art, as stated in the Office Action, and the rejection is appropriate.

With regard to Claim 11, Applicant's contention that the references "teach away" from the claim limitations is not correct. Since both are n-type implants, implant conditions and anneal conditions can be adjusted to yield essentially the same results, as discussed in detail in the Office Action.

With regard to Claims 12 and 13, the argument is not germane since the reference reads upon the claim.

Conclusions

23. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thomas Magee
July 14, 2004